Challenges & Solutions

in Prototyping 5G Radio Access Networks

David Squires, VP Business Development

BEEcube, A National Instruments Company

Agenda

- 5G, What Is It?
- Key Innovations/Enhancements Needed
- Ideal 5G Wireless Prototyping Platform

What Is 5G

- 1000x capacity
- 100 billion devices
- 10Gb/s to individual users
- Low latency connectivity
- Deployment starting 2020
- Combine LTE, WiFi, new spectrum, new air interfaces

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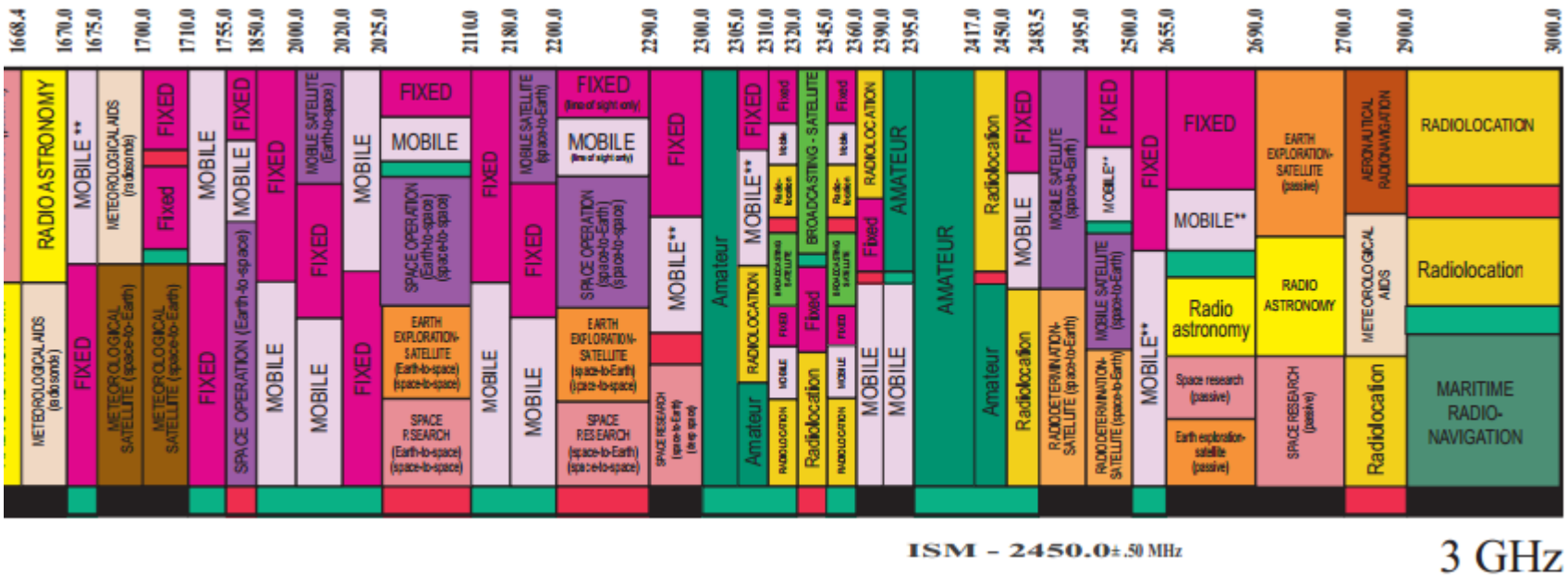
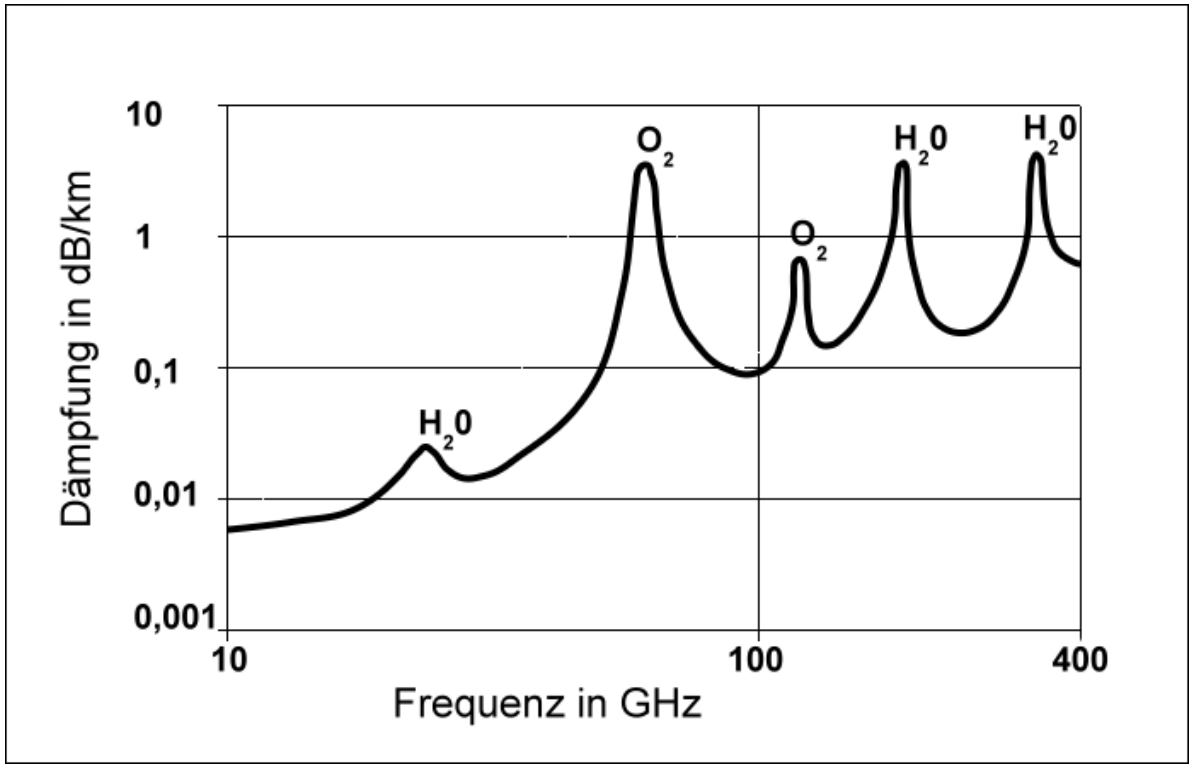
Spectrum Below 10GHz Is Jammed!

Existing US Bandplan Below 3GHz



mmWave – The New Frontier



Challenges

- Antennas
- Transmitters
- Receivers
- Absorption

Source: Wikipedia

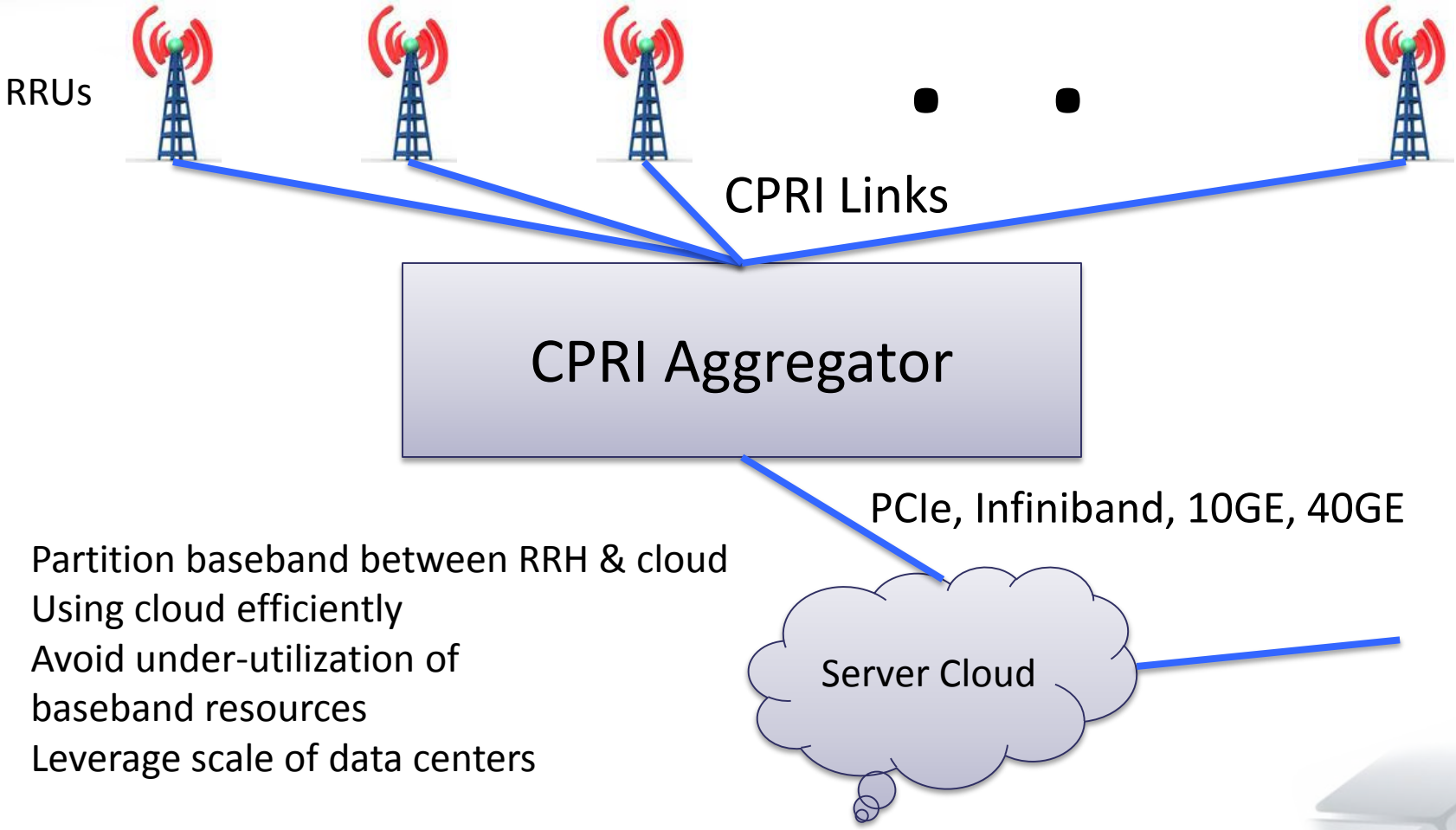
New Air Interfaces

- Modulation
  - Filter Bank Multi Carrier (FBMC)
  - Universal Filtered Multi Carrier (UFMC)
  - Generalized Frequency Div Multiplexing (GFDM)
- Coding
  - Reed Solomon, Turbo
  - Low Density Parity Check (LDPC)

Massive MIMO

- 128x128 and beyond
- Position peaks and nulls
- Increase channel capacity
- Increase # antennas in UE
- Adaptive systems can better utilize multi-path

C-RAN



- Partition baseband between RRH & cloud
- Using cloud efficiently
- Avoid under-utilization of baseband resources
- Leverage scale of data centers

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Open Programming Model

- LabView
- MATLAB
- Simulink
- C/C++
- VHDL
- Verilog

Real Time Operation

- Channel models not accurate
  - MIMO, new frequencies
- Channel changes in ms to seconds
- MUST test in real time to observe issues
- Field trials
  - 1000’s of hours of testing
  - Identify and test all corner cases

Scalable

Application	Tb/s	TMAC/s+
20MHz LTE Channel	0.001	0.001
200MHz Channel	0.01	0.01
1GHz Channel	.05	0.05
1GHz 3x sector	0.15	0.15
1GHz 8x8 MIMO 3x sector	10	10
1GHz 128x128, 3 sector	~1000*	~1000*

+ Assume 100 users per channel

* Assume increased efficiencies in high order MIMO

Efficient Connection to Cloud

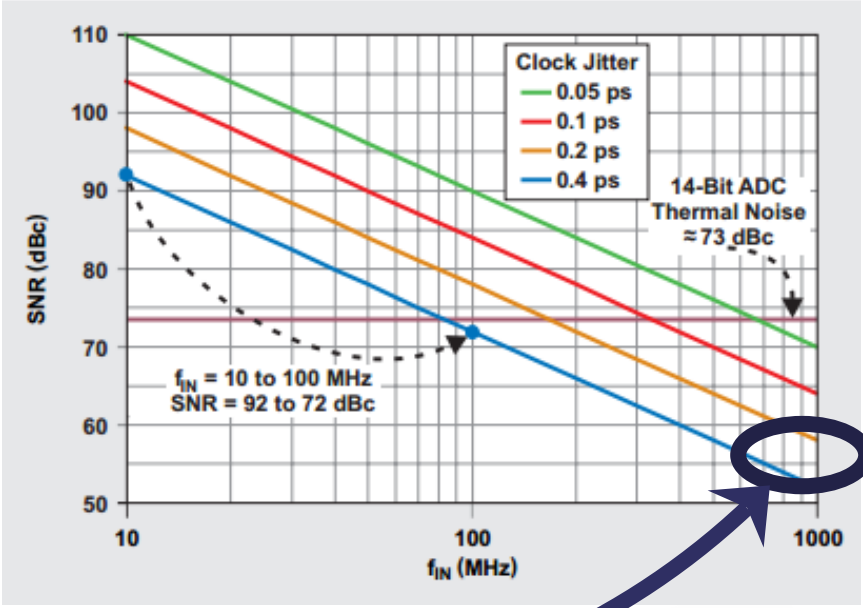
- Physical interface
  - GE
  - 10GE
  - 40GE
  - PCIe Gen3
- Standard hardware
  - XEON cards
  - Telecom cabinets
  - Industry compatible, fits in the ecosystem

Extract Embedded Clocks

- Macrocell base stations typically use GPS as master clock
- Small cells often located indoors
  - Access to GPS not possible
  - Must still be synchronized to network
  - Extract the clock from CPRI or synchronous Ethernet
- Large systems must be phase coherent
  - Extracted clock provides phase coherency across system
- Must remove jitter in recovered clocks

Clock Jitter <300fs

- 12 bit ADC -> theoretical SNR 72dB
- In practice, lose ~2 bits -> ~ 60dB
- In practice, need 55dB for good operation
- @1GHz BW
  55dB-> 300fs clock jitter



Source: Texas Instruments App Note: Clock Jitter Analyzed in Time Domain

5G Prototype Platform Checklist

- Open programming model
- Able to migrate designs to production
- Scalable – UE to 3 sector MIMO basestation
- Connectivity – scalable to minimum 10Tb/s
- DSP – scalable to 50TMAC/s
- Real-Time operation
- Extract embedded clocks
- Clock jitter < 300fs
- Ease of use

BEEcube Platforms – Check Us Out

BEE7	megaBEE	nanoBEE
		
Ultimate Performance Field Deployable	Massive MIMO	Low-cost Terminal Emulator

Terra MACs	5	1	0.5
Digital Gbits/sec I/O	1,100	160	80
# FMC Card Slots	4	2	1
Clock Jitter	300fs	300fs	300fs
# MIMO Ch/Blade	4 - 16	8	2-4
# MIMO Ch/Rack	144 - 576	256	N/A

Thank You!

David Squires, VP Business Development
Email: david@beecube.com
Cell: +1 408 834 5878